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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/759,603	01/16/2001	Joerg Drescher	225/49512	9440
23911	7590	11/17/2005		
CROWELL & MORING LLP INTELLECTUAL PROPERTY GROUP P.O. BOX 14300 WASHINGTON, DC 20044-4300				
			EXAMINER STEVENS, THOMAS H	
			ART UNIT 2123	PAPER NUMBER

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/759,603	<b>Applicant(s)</b> DRESCHER ET AL.	
	<b>Examiner</b> Thomas H. Stevens	<b>Art Unit</b> 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 August 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-3, 7-11 and 13-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 7-11 and 13-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 May 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

1. Claims 1-20 were previously examined.
2. Claims 4-6, 12, were cancelled.
3. Claims 1-3, 7-11, 13-20 were examined and rejected.

***Section I: Non-Final Rejection (2<sup>nd</sup> Office Action)***

***New Examiner***

4. Tom Stevens is presiding over the prosecution in place of Mary Hogan.

***Drawing Objection***

5. Relative to page 10, line 24, element 26 is absent from all drawings.  
Replacement drawings or amendment of the specification is required.

***Joint Inventors Common Ownership Presumed***

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

***Claim Rejections - 35 USC § 112***

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

**MPEP 2106:**

The subject matter of a properly construed claim is defined by the terms that limit its scope. It is this subject matter that must be examined. As a general matter, the grammar and intended meaning of terms used in a claim will dictate whether the language limits the claim scope. Language that suggests or makes optional but does not require steps to be performed or does not limit a claim to a particular structure does not limit the scope of a claim or claim limitation. The following are examples of language that may raise a question as to the limiting effect of the language in a claim: (A) statements of intended use or field of use, (B) "adapted to" or "adapted for" clauses, (C) "wherein" clauses, or (D) "whereby" clauses. This list of examples is not intended to be exhaustive.

6. Claims 2 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The word "substantially" and "adapted", respectively, is vague within the context of the claim.

***Claim Rejections - 35 USC § 103***

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1-3,7-9, 13-17, 19 and 20 are rejected under 35 U.S.C. 103 (a) as obvious by Wilamowski ("VLSI Analog Multiplier/Divider Circuit" (1998)) in view of Hyduke (US Patent 5,479,355 (1995)). Wilamowski teaches VLSI analog multiplier divider circuit using SPICE simulation (pg.495, left column) with a four-quadrant amplifier (pg. 496, right column, lines 5-6); but doesn't teach simulating actuators/sensors in real-time. Hyduke teaches a system and method for a closed loop operation (abstract) that encompasses simulation of electronic devices, in real-time (column 12, lines 21-22), such as actuators and sensors (columns 9-10, lines 67, 1-7, respectively); but doesn't teach simulation of circuits encompassing four-quadrant amplifiers.

At the time of invention, it would have been obvious to one of ordinary skill in the art to combine Wilamowski and Hyduke to resolve the urgent need to provide a more general, integrated, easier to use and less costly design emulation, simulation acceleration and hardware modeling tool (Hyduke: column 3, lines 16-19) while increasing versatility to many intelligent systems of industrial electronics (Wilamowski: abstract, last sentence).

Claim 1. An apparatus for simulating an electrical sensor/actuator component, (Hyduke: columns 9-10, lines 67, 1-7, respectively) comprising: a drive module including a model of the sensor/actuator component, said drive module generating interface signals in accordance with signals of said sensor/actuator component being simulated, said drive module further including at least one signal interface (Hyduke: abstract) with each one of said at least one signal interface (Hyduke: abstract) including and output stage with a four quadrant amplifier (Wilamowski: pg. 496, right column, lines 5-6) which functions to one of receiver or output power and with each of said at least one signal interfaces being associated with a respective connection pin (Hyduke: column 8, lines 25-33) which is driven by real-time signals (Hyduke: column 12, lines 20-24) from said drive module and wherein said at least one signal interface (Hyduke: abstract) generates, for each said interface connection pin, (Hyduke: column 8, lines 25-33) one of said interface signals corresponding to the electrical signals of said sensor/actuator component; wherein each of said at least one signal interface includes a control/regulation circuit for directing current or energy of said generated interface signals in a direction either towards (Hyduke: column 11, lines 21-30) said at least one signal interface (Hyduke: abstract) or away from said at least one signal interface whereby a sensor or an actuator can be optionally simulated.

Claim 2. An apparatus for simulating an electrical sensor/actuator component, (Hyduke: columns 9-10, lines 67, 1-7, respectively) comprising: a drive module including a model

of the sensor actuator component, said drive module generating interface signals in accordance with signals of said sensor/actuator component being simulated, said drive module further including a plurality of signal interfaces (plurality of lines equates to plurality of signals; Hyduke: column 4, lines 40-44) with each of said being associated with a respective connection pin which is driven by a real-time signals (Hyduke: column 12, lines 20-24) said drive module and wherein said plurality of signal interfaces (plurality of lines equates to plurality of signals; Hyduke: column 4, lines 40-44) generates, for each said interface connection pin, one of said an interface signals corresponding to the electrical signals of said sensor/actuator component; a main printed board having one insertion location (examiner establishes equivalence between main board and functional board testing: column 10, lines 53-57) for each interface connection for each of said interface pins and wherein one of said signal interfaces is provided for each location; wherein said apparatus includes modular construction in order to provide a separate signal interface for each interface component and wherein each of said plurality of signal interfaces (plurality of lines equates to plurality of signals; Hyduke: column 4, lines 40-44) are of substantially identical construction to provide generation of logic signals for a data line.

Claim 3. The apparatus according to Claim 1, wherein said drive module further includes means for calculating mathematical modules (analog to digital event represents a complex mathematical event; Hyduke: column 9, lines 44-52) for driving said at least one signal interface and wherein said module generates said real-time

signals (Hyduke: column 12, lines 20-24) in order to obtain said interface signals in accordance with the simulated sensor/actuator (Hyduke: columns 9-10, lines 67, 1-7, respectively) components at the interface connection pins.

Claim 7. The apparatus according to Claim wherein said drive module comprises a computer for providing an equivalent circuit (Inherent: well known within the art of circuit design) of the sensor/actuator component as said model.

Claim 8. The apparatus according to Claim 1, wherein said model of said drive module is adapted to signals required at an interface connection pin by utilizing specific parameters (equivalent to pin assignments; (Hyduke: column 8, lines 25-33).

Claim 9. The apparatus according to Claim further comprising a fault simulation module for generating one of a line interruption (Hyduke: column 4, lines 45-53) and a short circuit (Ohm's Law).

Claim 13. The apparatus according to Claim 2, wherein said drive module further includes means for calculating mathematical modules for driving said at least one signal interface (Hyduke: abstract) and wherein said module generates said real-time signals in order to obtain said interface signals in accordance with the simulated sensor/actuator (Hyduke: columns 9-10, lines 67, 1-7, respectively) components at the interface connection pins.



Claim 14. The apparatus according to Claim 2, further including a main printed circuit board having one insertion location for each interface connection for each of said interface pins and wherein one of said signal interfaces (Hyduke: abstract) is provided for each insertion location.

Claim 15. The apparatus according to Claim 2, wherein each of said signal interfaces (Hyduke: abstract) has an output stage.

Claim 16. The apparatus according to Claim 2, wherein said output stage is a four-quadrant amplifier, (Wilamowski: pg. 496, right column, lines 5-6) which can function to output power or to receive power.

Claim 17. The apparatus according to Claim 2, wherein said drive module comprises a computer for prodding an equivalent circuit (Inherent: well know within the art of circuit design) of the sensor/actuator component (Hyduke: columns 9-10, lines 67, 1-7, respectively) as said model.

Claim 19. The apparatus according to Claim 2, further comprising a fault simulation module for generating one of a line interruption (Hyduke: column 4, lines 45-53) and a short circuit (Ohm's Law).

Claim 20. The apparatus according to Claim 2, wherein each of said signal interfaces (Hyduke: abstract) has a regulating circuit for adjusting one of voltage and current to a value specified by said model.

12. Claims 10,11,18 are rejected under 35 U.S.C. 103 (a) as obvious by Wilamowski ("VLSI Analog Multiplier/Divider Circuit" (1998)) in view of Hyduke (US Patent 5,479,355 (1995)) and in further view of Hanf et al., (US Patent 6,438,462 (2002)). Wilamowski teaches VLSI analog multiplier divider circuit using SPICE simulation (pg.495, left column) with a four-quadrant amplifier (pg. 496, right column, lines 5-6); but doesn't teach simulating actuators/sensors in real-time. Hyduke teaches a system and method for a closed loop operation (abstract) that encompasses simulation of electronic devices such as actuators and sensors (columns 9-10, lines 67, 1-7, respectively); but doesn't teach simulation of four-quadrant amplifiers. Hanf teaches a semiconductor circuit for an electronic unit having at least on microcontroller (abstract) with application specific sensors, drive requisite actuators, regulators circuit feedback but doesn't teach simulating or simulation of circuit encompassing four-quadrant amplifiers.

At the time of invention, it would have been obvious to one of ordinary skill in the art to combine Wilamowski, Hyduke and Hanf to resolve the urgent need to provide a more general, integrated, easier to use and less costly design emulation, simulation acceleration and hardware modeling tool (Hyduke: column 3, lines 16-19) while increasing versatility to many intelligent systems of industrial electronics (Wilamowski: abstract, last sentence) for cost-effectiveness (Hanf: column 12, lines 54-58).

Claim 10. The apparatus according to Claim 1, wherein each of said signal interfaces (Hyduke: abstract) has a regulating circuit (Hanf: column 52, lines 16-19) for adjusting one of voltage and current to a value specified by said model.

Claim 11. The apparatus according to Claim 10, wherein said regulating circuit (Hanf: column 52, lines 16-19) includes a feedback arrangement (Hanf: column 33, lines 15-16) to the drive module in order to provide actual values of regulated variables to said model.

Claim 18. The apparatus according to Claim 2, wherein said model of said drive module (assuming actuator is a module; Hanf: column 2, lines 42-43) is adapted to signals required at an interface (Hyduke: abstract) connection pin by utilizing specific parameters.

### ***Citation of Relevant Prior Art***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Becerra et al., "Four-Quadrant Brushless ECM Drive with Integrated Current Regulation" IEEE. 1992. pg. 833-841: method of regulating the phase currents in brushless electronically commutated motor during four-quadrant operations.
- Bachmayer et al., "An Accurate Four-Quadrant Nonlinear Dynamical Model for Marine Thrusters: Theory and Experimental Validation" 2000. pg. 146-159: teaches two improvements in finite-dimensional non-linear dynamic modeling of marine thrusters.

- Walker-J., "Four Quadrant Amplifier" 1995 IEEE pg. 947-951 : teaches a switching mode amplifier base on the flyback topology.
- Veijola et al., "Dynamic Modelling and Simulation of Microelectromechanical Devices with a Circuit Simulation Program" 1998 Helsink Univ. of Technolgy. pg.245-250: teaches simulation blocks of micromechanical sensors and actuators modeling dynamic electromechanical and fluidic operation.
- Wilamowski-B., "VLSI Analog Multiplier/Divider Circuit" 1998 IEEE pg. 493-496: teaches a new accurate CMOS multiplier/divider circuit.
- Fedder et al., "NODAS 1.3—Nodal Design of Actuators and Sensors" Carnegie Mellon Univ. 1998 pg. 1-8: teaches a hierarchical design and nodal simulation of microelectromechanical systems.
- US Patent 6,208,954: teaches a method and apparatus for sequencing the execution of a simulation system comprising at least two subsystem simulators.
- US Patent 6,262,544: The present invention relates to four quadrant motor operation, and more particularly, to a circuit and associated method for recreating actual motor current from sensed bus current information.
- US Patent 4,300,205: The invention teaches an apparatus for simulating the operating characteristics of an automobile engine. The ignition system of the engine is electrically simulated and an electrical signal representative of engine revolutions per minute under various engine operation conditions is generated. A transfer function derived for the engine is implemented to control generation of the electrical signal. Engine acceleration and deceleration is simulated.
- US Patent 4,463,605: To simulate, for testing purposes, the subsystems of an aircraft that electrohydraulically position the movable control surfaces of an aircraft, circuitry is provided for receiving input control signals, generated, for example, by an autopilot, and for transforming such signals into

electrical output signals that are the analogs of signals produced by linear variable differential transformers (LVDT) feedback devices that track the actual movements and positions of the aircraft control surfaces. The relatively slow acting hydraulic components of the aircraft control subsystems are simulated by integrating circuitry and the resulting integrated signals are used to modulate an AC reference signal, which is then applied to the primaries of isolation transformers, the secondaries of which produce the simulated, analog LVDT feedback signals and also present a load impedance to the autopilot that closely matches the output windings of the simulated LVDTs.

## ***Section II: Response to Applicants' Arguments***

### ***Specification Objection***

11. Applicants are thanked for responding to this issue. Objection is withdrawn.

### ***112 2<sup>nd</sup> Rejection***

12. Applicants are thanked for responding to this issue. Rejection is withdrawn.

### ***102(b)***

13. Applicant's arguments, see pages 8-10, filed 8/26/05, with respect to the rejections of claims 1-20 under 35 U.S.C. 102(b) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, new grounds of rejection are made in view of Wilamowski, Hyduke and Hanf.

***Correspondence Information***

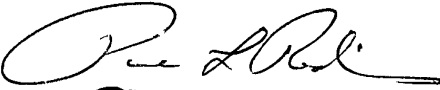
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm EST).

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Leo Picard ((571) 272-3749). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).

November 5, 2005

TS

  
Paul L. Rodriguez 11/14/05  
Primary Examiner  
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